AMENDMENTS TO THE CLAIMS

1. (Currently Amended) An arrangement comprising:

a first semiconductor chip configured to transmit load control data and pilot data on a single line;

a second semiconductor chip coupled to the first semiconductor chip and configured to receive the load control data and the pilot data; and

a plurality of electrical loads coupled to the second semiconductor chip;

wherein the second semiconductor chip is configured to:

a) drive the plurality of electrical loads based on a timing that is defined by the load control data,

b) transmit to the first semiconductor chip diagnostic data, which represent at least one of a plurality of states of the second semiconductor chip and events which occur in the second semiconductor chip, and

c) control a transmission rate of the diagnostic data as prescribed by the pilot data.

2. (Original) The arrangement as claimed in claim 1, wherein the first semiconductor chip is a program-controlled unit.

3. (Original) The arrangement as claimed in claim 1 wherein the second semiconductor chip is a power chip.

4. (Previously Presented) The arrangement as claimed in claim 1, wherein the diagnostic data are

transmitted in time with a transmission clock signal generated in the second semiconductor chip, and the transmission clock signal is not transmitted to the first semiconductor chip.

5. (Previously Presented) The arrangement as claimed in claim 1, wherein the transmission rate is prescribed by transmitting a division factor, and the second semiconductor chip divides the frequency of a transmission clock signal received from the first semiconductor chip by the division factor, and transmits the diagnostic data to the first semiconductor chip in time with the resultant transmission signal.

6. (Previously Presented) The arrangement as claimed in claim 5, wherein the transmission clock signal transmitted to the second semiconductor chip represents the transmission clock which is used by the first semiconductor chip to transmit the load control data or the pilot data to the second semiconductor chip.

7. (Previously Presented) The arrangement as claimed in claim 6, wherein the diagnostic data are transmitted in units of frames and each frame starts with a start bit having a prescribed value and ends with one or two stop bits having prescribed values.

8. (Previously Presented) The arrangement as claimed in claim 1, wherein the first semiconductor chip ascertains a phase of the diagnostic data by oversampling the diagnostic data.

9. (Previously Presented) The arrangement as claimed in claim 1, wherein the diagnostic data are transmitted via a line, which transmits neither the load control data nor the pilot data.

10. (Original) The arrangement as claimed in claim 1, wherein the load control data and the pilot data are transmitted via a transmission channel.

11. (Previously Presented) The arrangement as claimed in claim 10, wherein the transmission channel comprises:

a transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip;

a data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal; and

a chip select line via which the first semiconductor chip transmits a chip select signal to the second semiconductor chip,

wherein said chip select signal indicates to the second semiconductor chip a start and end of data transmission intended for the second semiconductor chip via the data line.

12. (Previously Presented) The arrangement as claimed in claim 1, wherein the load control data and the pilot data are transmitted in units of frames and are transmitted using time-division multiplexing.

13. (Previously Presented) The arrangement as claimed in claim 12, wherein the first semiconductor chip defines time windows of constant length and transmits in each time window either a load control data frame or a pilot data frame or no data.

14. (Previously Presented) The arrangement as claimed in claim 13, wherein the first semiconductor chip transmits no further load control data frames for a respective length of n time windows after transmission of a load control data frame,

wherein $n \geq 0$ and n can be set by a user of the arrangement.

15. (Previously Presented) The arrangement as claimed in claim 14, wherein a pilot data frame can be transmitted only in a time window in which no load control data frame is transmitted.

16. (Original) The arrangement as claimed in claim 13, wherein transmission of the pilot data has priority when load control data and pilot data are awaiting transmission simultaneously.

17. (Previously Presented) An arrangement comprising

a first semiconductor chip and a second semiconductor chip connected thereto,

where the second semiconductor chip is additionally connected to electrical loads and drives these electrical loads on the basis of a timing which is defined by load control data,

where the first semiconductor chip transmits via a transmission channel to the second semiconductor chip the load control data and pilot data which control the second semiconductor chip,

where the transmission channel comprises:

a first transmission clock line via which the first semiconductor chip transmits a transmission clock signal to the second semiconductor chip;

a second transmission clock line via which the first semiconductor chip transmits an inverse of the transmission clock signal to the second semiconductor chip;

a first data line via which the first semiconductor chip transmits the load control data and the pilot data to the second semiconductor chip in time with the transmission clock signal;

a second data line via which the first semiconductor chip transmits an inverse of the load control data and an inverse of the pilot data to the second semiconductor chip; and

a chip select line via which the first semiconductor chip transmits a chip select signal to the

second semiconductor chip,

wherein said chip select signal signals to the second semiconductor chip a start and end of transmission of data intended for the second semiconductor chip via the data line,

where the second semiconductor chip transmits to the first semiconductor chip diagnostic data which represent at least one of states prevailing in the second semiconductor chip and events which occur in the second semiconductor chip,

wherein the first semiconductor chip includes means for transmitting appropriate pilot data to the second semiconductor chip, and the second semiconductor chip includes means for controlling a transmission rate by which the diagnostic data is transmitted to the first semiconductor chip in accordance with the appropriate pilot data.

18. (Previously Presented) The arrangement as claimed in claim 17, wherein output drivers on the first semiconductor chip, which output the load control data, the pilot data and the transmission clock signal, are LVDS drivers or other special drivers whose use allows electromagnetic interference to be kept down.

19. (Previously Presented) The arrangement as claimed in claim 1, wherein the first semiconductor chip has a plurality of output drivers configured to output the load control data, the pilot data and the transmission clock signal.

20. (Previously Presented) The arrangement as claimed in claim 17, wherein output drivers on the first semiconductor chip, which output the load control data, the pilot data and the transmission clock signal, are special drivers configured to minimize electromagnetic interference.